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Docket No.: TESSERA 3.0-320

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kang et al.

Application No.: Not Yet Assigned Group Art Unit: N/A

Filed: Herewith

Examiner: Not Yet Assigned

For: ASSEMBLIES HAVING STACKED SEMICONDUCTOR CHIPS AND METHODS OF MAKING SAME

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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Dear Sir:

It is respectfully requested that the references listed on the enclosed form be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each non-U.S. Patent and/or U.S. published patent application reference is enclosed. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited references are legally available prior art or that the same are pertinent or material.

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Dated: September 5, 2003

Respectfully submitted,

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S	TATEMEN1	BY A	PPLICANT	First Named Inventor	Teck-Gyu Kang	
	(1100 00 00 00			Art Unit	N/A	
	(Use as many sheets as necessary)			Examiner Name	Not Yet Assigned	
Sheet	1	of	1	Attorney Docket Number	TESSERA 3.0-320	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number-Kind Code ² (if known)				
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
	CA	BANG, ET AL., U.S. Provisional Patent Application Serial No. 60/403,939, filed Aug. 16, 2002.	 		
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